

Amendments to the Specification

Please replace paragraphs [48], [49] and [50] with the following amended paragraphs:

FIG. 4A ~~show~~shows a first column block 100a of the screen save modes implemented for the column block unit, and FIG. 4B shows the last column block 100d of the screen save modes implemented for the column block unit.

As shown in FIGs. 4A and 4B, the screen save mode is sequentially applied to each of the column blocks 100a-100d, and the corresponding columns within each the currently chosen column block (100a in Fig. 4A and 100d in Fig. 4B) are sequentially turned on while columns corresponding to the other column blocks (100b and 100c) are turned off, except for pixels that are displaying display data. These steps are repeated until the screen save modes of all column blocks 100a-100d are completed.

The control unit 40 confirms whether the display data applied to the display panel 10 are uniformly maintained for a predetermined time. If the display data are uniformly maintained for a predetermined time, the control unit 40 divides the pixels of the display panel 10 into at least one pixel column block 100a-100d. Then, the screen save modes are sequentially performed on the pixel column-block blocks 100a-100d.

Please replace paragraphs [55], [56] and [57] with the following amended paragraphs:

FIG. 5A show a first row block 200a of the screen save modes implemented for the row block unit, and FIG. 5B shows the last row block 200d of the screen save modes implemented for the row block unit.

As shown in FIGs. 5A and 5B, the screen save mode is sequentially applied to each of the row blocks 200a-200d, and the corresponding columns within each the currently chosen row block (200a, Fig. 5A and 200d in Fig. 5B) are sequentially turned on while rows

corresponding to the other row blocks (200b and 200c) are turned off, except for pixels that are displaying display data. These steps are repeated until the screen save modes of all row blocks 200a-200d are completed.

The control unit 40 confirms whether the display data applied to the display panel 10 are uniformly maintained for a predetermined time. If the display data are uniformly maintained for a predetermined time, the control unit 40 divides the pixels of the display panel 10 into at least one pixel row block 200a-200d. Then, the screen save modes are sequentially performed on the pixel row ~~block~~ blocks 200a-200d by the control unit 40.

Please replace paragraphs [62], [63] and [64] with the following amended paragraphs:

FIG. 6A show a first $N1 \times M1$ pixel block 300a of the screen save modes implemented for a certain pixel block unit, and FIG. 6B shows the last $N1 \times M1$ pixel block 300h of the screen save modes implemented for the certain pixel block unit.

Pixels of ~~one the currently chosen~~ $N1 \times M1$ pixel block (300a in Fig. 5A and 300h in Fig. 6B) are turned on while pixels of the other $N \times M$ pixel blocks 300b-300g are turned off, except for pixels that are displaying display data. These steps are repeated until the screen save modes of all $N1 \times M1$ pixel blocks 300a-300h are completed.

The control unit 40 confirms whether the display data applied to the display panel 10 are uniformly maintained for a predetermined time. If the display data are uniformly maintained for a predetermined time, the control unit 40 divides the pixels of the display panel 10 into at least one $N1 \times M1$ ($N1$ and $M1$ are positive integers) pixel row block 300a-300h. The screen save mode is then sequentially performed on the $N1 \times M1$ pixel ~~block~~ blocks 300a-300h.

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Please replace paragraph [72] with the following amended paragraphs:

In FIGs. 8A and 8B, the control unit 40 confirms whether the display data applied to the display panel 10 are uniformly maintained for a predetermined time. If the display data are uniformly maintained for a predetermined time, the control unit 40 divides the pixels of the display panel 10 into at least one pixel block 400. Then, the control unit 40 sequentially applies the screen save mode data to the at least one pixel block 400.